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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,644	03/23/2004	Vahid Goudarzi	CE12694JME	2480

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EXAMINER
SANDVIK, BENJAMIN P

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/806,644	GOUDARZI, VAHID	
	Examiner	Art Unit	
	Ben P. Sandvik	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *16 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-17 have been considered but are moot in view of the new ground(s) of rejection.

Upon further consideration, the Suppelsa reference does teach the limitations of the independent claims. More precisely, the Suppelsa reference teaches a conductive shield track and a solder cladding on said track as describing below.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 are rejected under 35 U.S.C. 102(b) as being anticipated by Suppelsa et al (U.S. Patent #5411199).

With respect to **claims 1 and 13**, Suppelsa teaches applying solder onto conductive areas on the substrate (Fig. 4, 302 and Col 2 Ln 57-58) including a conductive shield track for at least one shield (Fig. 2, track 112 on substrate 110), placing components onto the conductive areas for the components (Fig. 4, 304 and Col 2 Ln 60), a first reflow step (Fig. 4, 306) to provide solder joints for the components and a selectively solder cladded area over the conductive shield

track (Col 3 Ln 23), applying flux to the shield (Col 3 Ln 10-13), placing the shield over the solder cladded area (Fig. 4, 314), reflowing the assembly (Fig. 4, 316).

With respect to **claim 2**, Suppelsa teaches cleaning the substrate after reflow (Fig. 4, 306 and Col 2 Ln 62-63).

With respect to **claim 7**, Suppelsa teaches the step of applying solder preforms onto conductive areas (Fig. 4, 302).

With respect to **claims 9 and 17**, Suppelsa teaches the steps of: circumscribing a predetermined area on the substrate with at least a portion of a metallized trace pattern (Fig. 2, 112); applying solder to the metallized trace portion (Fig. 4, 302); placing components on portions of the metallized trace pattern (Fig. 4, 304); reflowing the solder to form substantially simultaneously a cladded trace pattern on a portion of the metallized trace pattern reserved for the shield (Col 3 Ln 23) and solder joints for the components (Col 2 Ln 63-64); placing the shield on the cladded trace pattern (Fig. 4, 314); and reflowing the substrate (Fig. 4, 316).

With respect to **claim 11**, Suppelsa teaches that the step of applying solder comprises applying a solder perform (Fig. 4, 302).

With respect to **claim 16**, Suppelsa teaches that the solder applied onto the conductive areas is solder perform (Fig. 4, 302).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suppelsa, in view of Lee (U.S. Patent #5620927).

With respect to **claim 3**, Suppelsa teaches all of the limitations of claim 1, but does not teach that the step of applying flux comprises the step of picking up the shield and dipping the shield into the flux. Lee teaches a process in which a component is dipped into flux before it is reflowed (Col 3 Ln 65-66). It would have been obvious to one of ordinary skill in the art at the time the invention was made apply the flux as in Suppelsa with the process of picking the shield up and dipping it into the flux as taught by Lee in order to remove oxides from the part to be connected by reflow.

Claims 4-6, 10, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suppelsa, in view of Degani et al (U.S. Patent #5346118).

With respect to **claim 4**, Suppelsa teaches all of the limitations of claim 1, but does not teach that the step of applying solder paste onto the conductive shield track comprises the step of over printing the solder to increase the solder volume to the conductive shield track to accommodate for the shield's non-coplanarity. Degani teaches a process of overprinting the solder paste in a

connection (Col 4 Ln 15-21). It would have been obvious to one of ordinary skill in the art at the time the invention was made to overprint the solder applied on the conductive shield track as taught by Degani in order to achieve a satisfactory joint volume.

With respect to **claim 5**, Suppelsa teaches all of the limitations of claim 1, but does not teach that the step of placing components comprises the step of placing surface mount components onto the substrate. Degani teaches the placing of surface mount components onto a substrate (Col 1 Ln 14). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the step in Suppelsa of placing components on the substrate to be placing surface mounted components on the substrate as taught by Degani in order to secure the components to the substrate.

With respect to **claim 6**, Suppelsa teaches all of the limitations of claim 1, but does not teach that the step of applying solder comprises the step of applying solder paste onto the conductive areas forming conductive pads for the components and the shield track. Degani teaches that a step of applying solder to form conductive pads for component to be connected comprises applying solder paste (Col 4 Ln 18). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply solder paste to form conductive pads as taught by Degani in the step of applying solder in Suppelsa in order to enhance the connection between the components and shield track and the substrate.

With respect to **claim 10**, Suppelsa teaches all of the limitations of claim 9, but does not teach that the step of applying solder comprises the step of applying solder paste to the metallized trace pattern. Degani teaches that a step of applying solder to form conductive pads for component to be connected comprises applying solder paste (Col 4 Ln 18). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply solder paste to form conductive pads as taught by Degani in the step of applying solder in Suppelsa in order to enhance the connection between the components and the substrate.

With respect to **claim 12**, Suppelsa teaches all of the limitations of claim 9, but does not teach that the step of placing components comprises the step of placing a semiconductor die on portions of the metallized trace pattern. Degani teaches mounted an integrated circuit package on a substrate (Fig. 1, 10). It would have been obvious to one of ordinary skill in the art at the time the invention was made to mount a semiconductor die as taught by Degani in order to use miniaturized electronic components to reduce the size of the package.

With respect to **claim 14**, Suppelsa teaches all of the limitations of claim 13, but does not teach that the step of placing components comprises the step of placing surface mount components onto the conductive areas. Degani teaches the placing of surface mount components onto a substrate (Col 1 Ln 14). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the step in Suppelsa of placing components on the

substrate to be placing surface mounted components on the conductive areas as taught by Degani in order to secure the components to the substrate.

With respect to **claim 15**, Suppelsa teaches all of the limitations of claim 13, but does not teach that the step of applying solder comprises the step of applying solder paste onto the conductive areas. Degani teaches that a step of applying solder to form conductive pads for component to be connected comprises applying solder paste (Col 4 Ln 18). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply solder paste to the conductive areas as taught by Degani in the step of applying solder in Suppelsa in order to enhance the connection between the components and shield track and the substrate.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suppelsa, in view of Liebman et al (U.S. Patent #5167361).

With respect to **claim 8**, Suppelsa teache all of the limitations of claim 1, but does not teach that the step of applying solder comprises the step of screen printing solder paste onto the conductive areas. Liebman teaches that a step of applying solder can comprise screen printing solder paste onto circuitry (Col 2 Ln 29-34). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the step of applying solder in Suppelsa comprise screen printing solder paste onto the conductive areas as taught by Liebman in

order to facilitate a connection between the components and the conductive areas.

NATHAN J. FLYNN
SUPERVISORY PATENT
TECHNOLOGY CE

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben P. Sandvik whose telephone number is (571) 272-8446. The examiner can normally be reached on Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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